P06226 PTUS.pdf

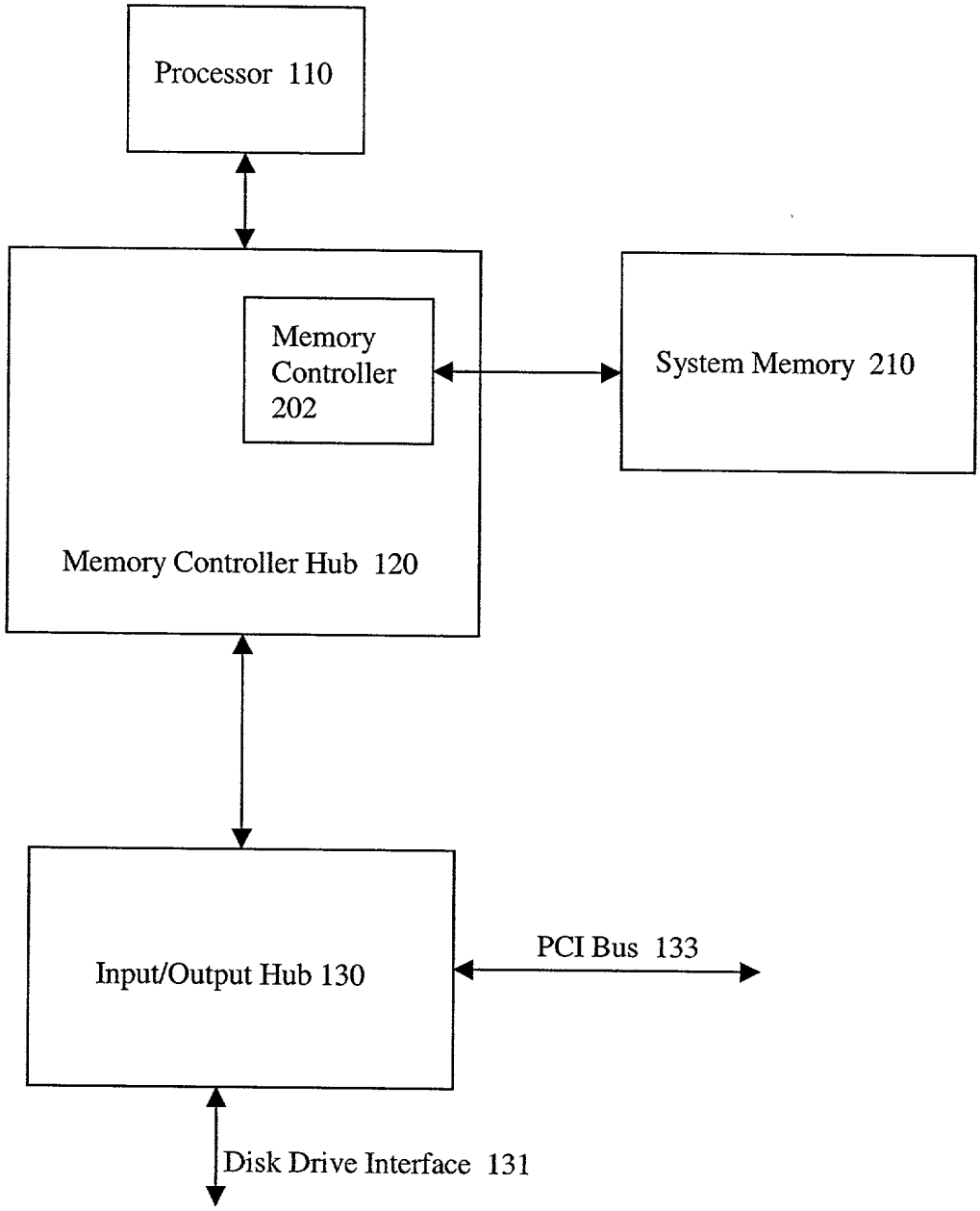

Figure 1

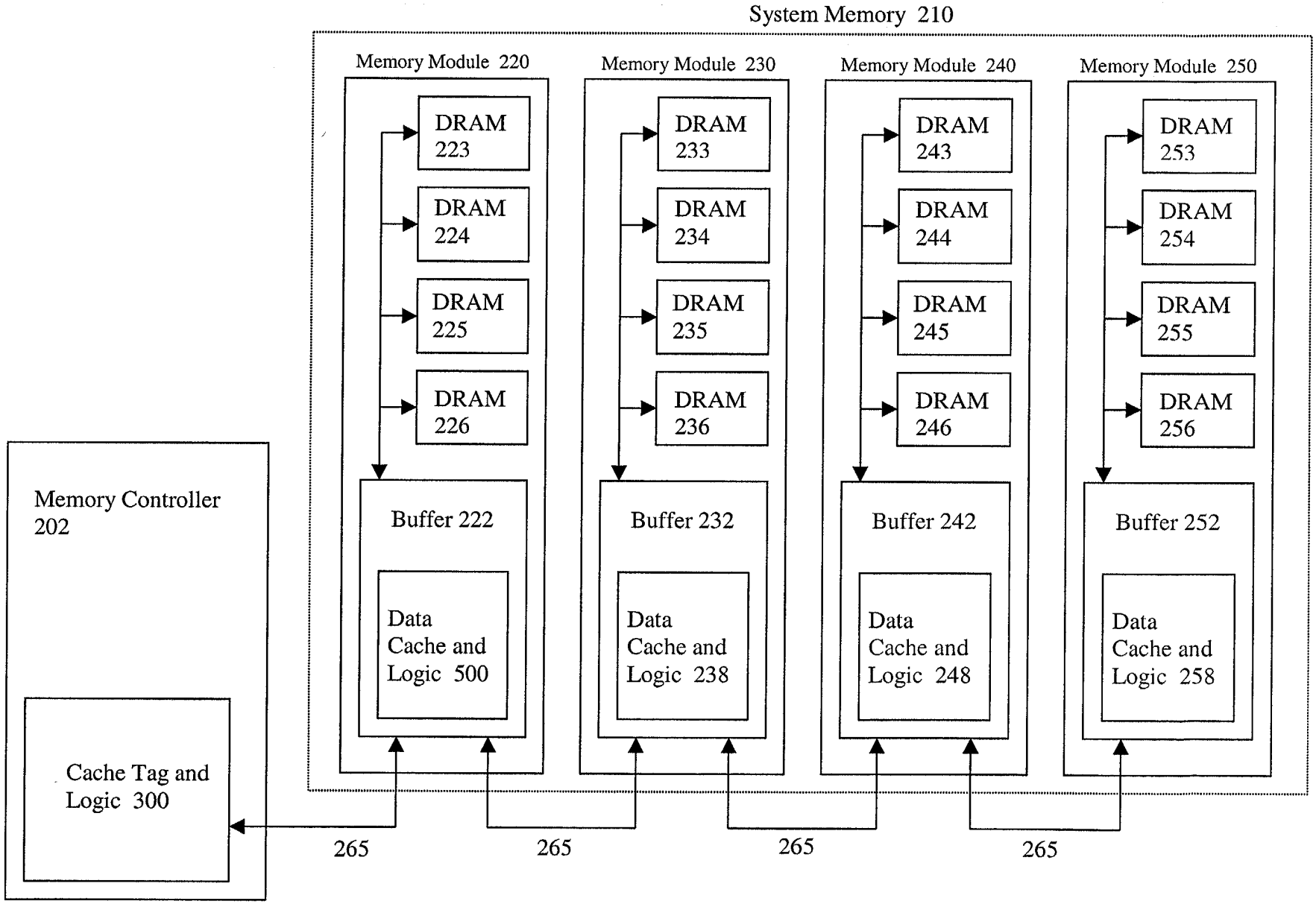
System Memory 210
Memory Module 220
Memory Module 230
Memory Module 240
Memory Module 250
DRAM 223
DRAM 224
DRAM 225
DRAM 226
DRAM 233
DRAM 234
DRAM 235
DRAM 236
DRAM 243
DRAM 244
DRAM 245
DRAM 246
DRAM 253
DRAM 254
DRAM 255
DRAM 256
Buffer 222
Buffer 232
Buffer 242
Buffer 252
Data Cache and Logic 500
Data Cache and Logic 238
Data Cache and Logic 248
Data Cache and Logic 258
Memory Controller 202
Cache Tag and Logic 300
265
265
265
265

Figure 2

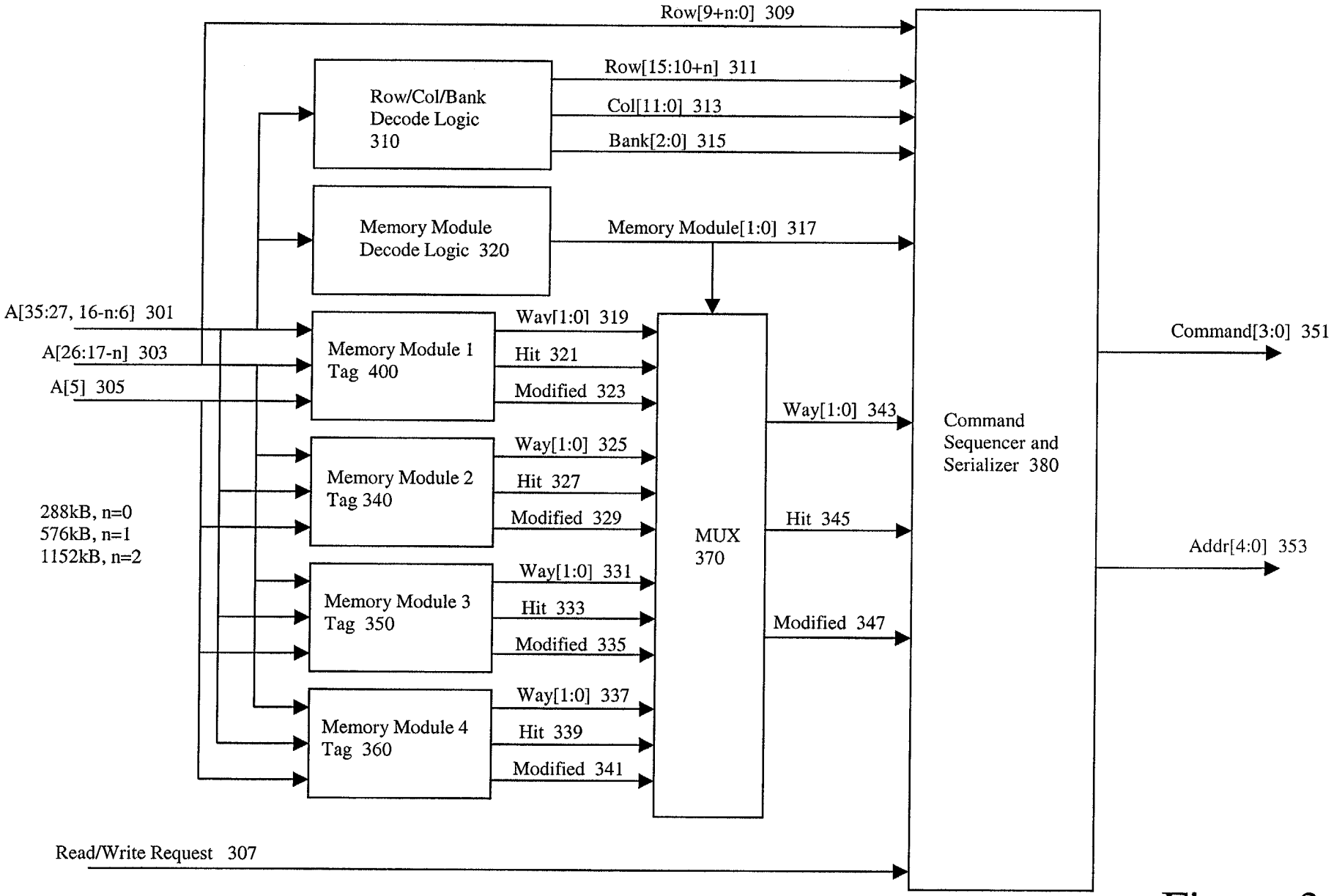
Row[9+n:0] 309
Row/Col/Bank Decode Logic 310
Row[15:10+n] 311
Col[11:0] 313
Bank[2:0] 315
Memory Module Decode Logic 320
Memory Module[1:0] 317
A[35:27, 16-n:6] 301
A[26:17-n] 303
A[5] 305
Memory Module 1 Tag 400
Way[1:0] 319
Hit 321
Modified 323
Memory Module 2 Tag 340
Way[1:0] 325
Hit 327
Modified 329
288kB, n=0
576kB, n=1
1152kB, n=2
Memory Module 3 Tag 350
Way[1:0] 331
Hit 333
Modified 335
Memory Module 4 Tag 360
Way[1:0] 337
Hit 339
Modified 341
MUX 370
Way[1:0] 343
Hit 345
Modified 347
Command Sequencer and Serializer 380
Command[3:0] 351
Addr[4:0] 353
Read/Write Request 307

Figure 3

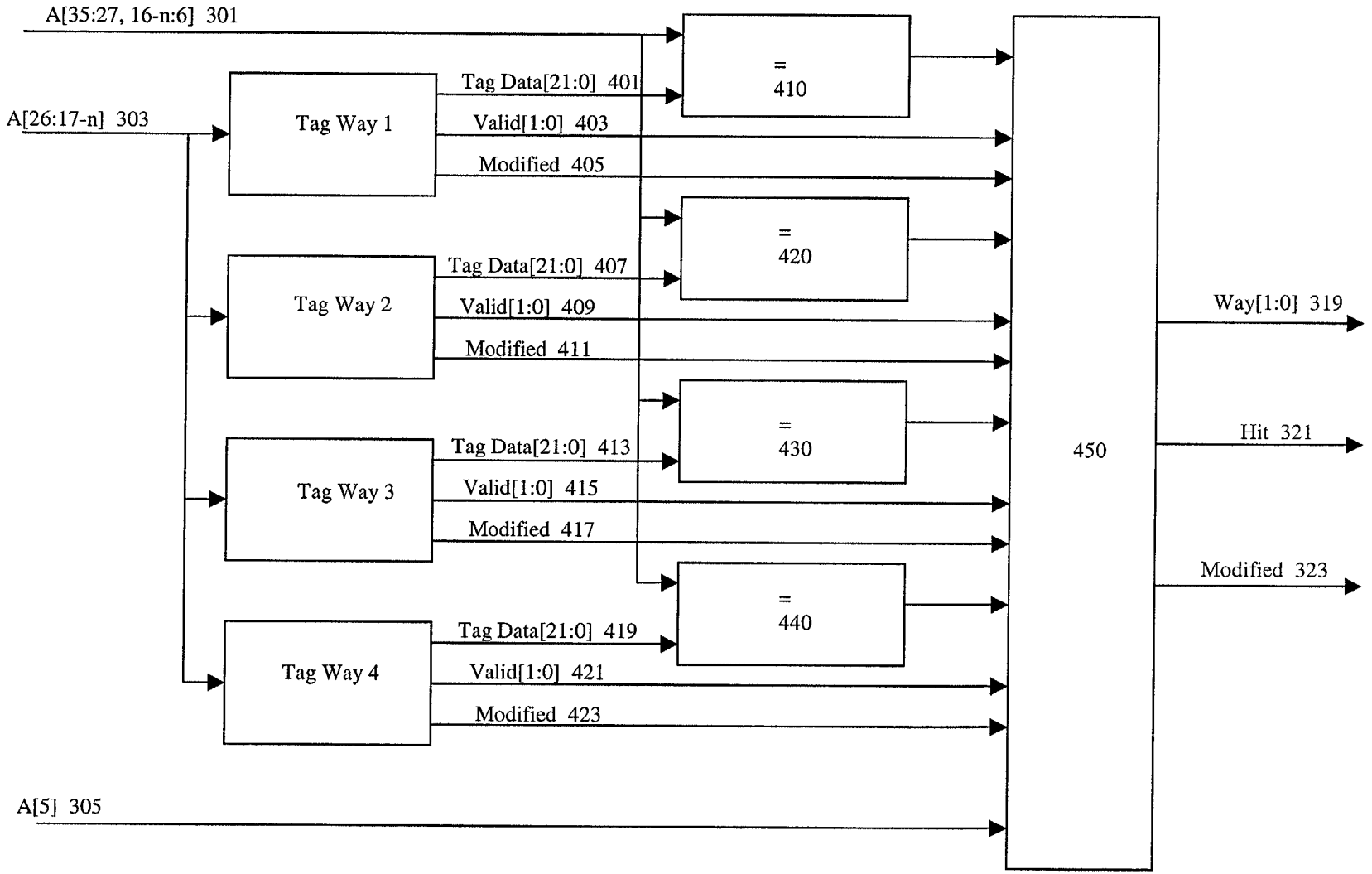
A[35:27, 16-n:6] 301
A[26:17-n] 303
Tag Way 1
Tag Data[21:0] 401
Valid[1:0] 403
Modified 405
=
410
Tag Way 2
Tag Data[21:0] 407
Valid[1:0] 409
Modified 411
=
420
Tag Way 3
Tag Data[21:0] 413
Valid[1:0] 415
Modified 417
=
430
Tag Way 4
Tag Data[21:0] 419
Valid[1:0] 421
Modified 423
=
440
450
Way[1:0] 319
Hit 321
Modified 323
A[5] 305

Figure 4

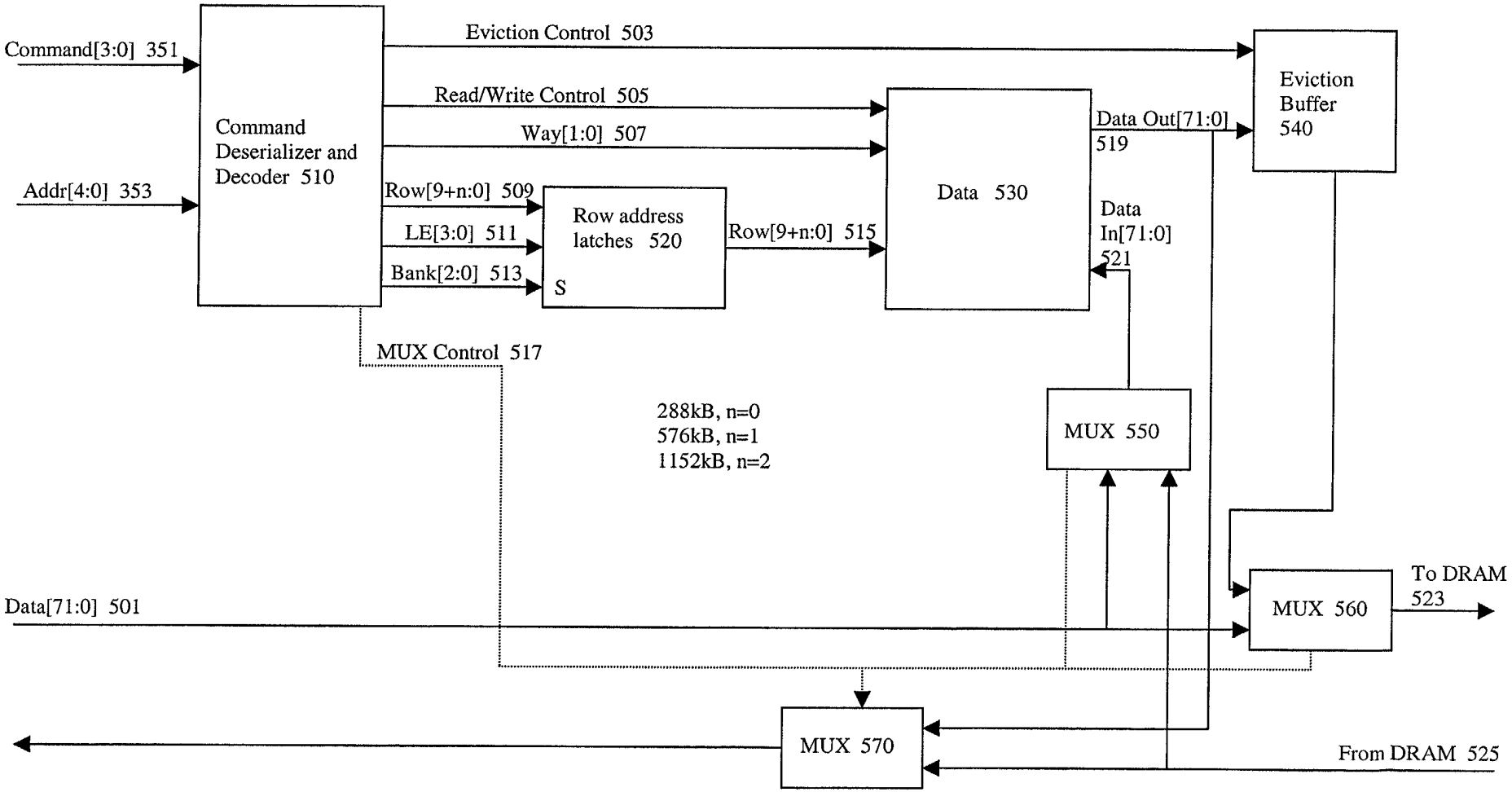
Command[3:0] 351
Addr[4:0] 353
Command Deserializer and Decoder 510
Eviction Control 503
Read/Write Control 505
Way[1:0] 507
Row[9+n:0] 509
LE[3:0] 511
Bank[2:0] 513
Row address latches 520
S
Row[9+n:0] 515
Data 530
Data Out[71:0] 519
Eviction Buffer 540
Data In[71:0] 521
MUX Control 517
288kB, n=0
576kB, n=1
1152kB, n=2
MUX 550
Data[71:0] 501
MUX 560
To DRAM 523
MUX 570
From DRAM 525

Figure 5